ANALOG DEVICES

Quad Precision, Low Cost, High Speed, BiFET Op Amp

AD713

FEATURES

Enhanced Replacement for LF347 and TL084

AC PERFORMANCE
1 μs Settling to 0.01% for 10 V Step
20 V/μs Slew Rate
0.0003% Total Harmonic Distortion (THD)
4 MHz Unity Gain Bandwidth

DC PERFORMANCE
0.5 mV max Offset Voltage (AD713K)
20 μV/°C max Drift (AD713K)
200 V/mV min Open Loop Gain (AD713K)
2 μV p-p typ Noise, 0.1 Hz to 10 Hz
True 14-Bit Accuracy
Single Version: AD711, Dual Version: AD712
Available in 16-Pin SOIC, 14-Pin Plastic DIP and Hermetic Cerdip Packages and in Chip Form
MIL-STD-883B Processing Available
Standard Military Drawing Available

APPLICATIONS

Active Filters
Quad Output Buffers for 12- and 14-Bit DACs
Input Buffers for Precision ADCs
Photo Diode Preamplifier Applications

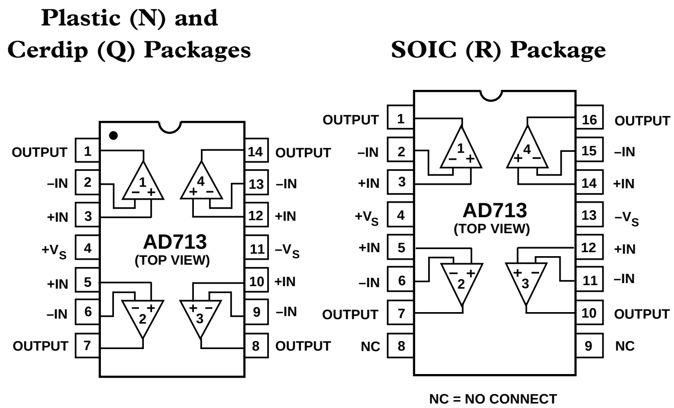
PRODUCT DESCRIPTION

The AD713 is a quad operational amplifier, consisting of four AD711 BiFET op amps. These precision monolithic op amps offer excellent dc characteristics plus rapid settling times, high slew rates, and ample bandwidths. In addition, the AD713 provides the close matching ac and dc characteristics inherent to amplifiers sharing the same monolithic die.

The single-pole response of the AD713 provides fast settling: 1 μs to 0.01%. This feature, combined with its high dc precision, makes it suitable for use as a buffer amplifier for 12- or 14-bit DACs and ADCs. It is also an excellent choice for use in active filters in 12-, 14- and 16-bit data acquisition systems. Furthermore, the AD713's low total harmonic distortion (THD) level of 0.0003% and very close matching ac characteristics make it an ideal amplifier for many demanding audio applications.

The AD713 is internally compensated for stable operation at unity gain and is available in seven performance grades. The AD713J and AD713K are rated over the commercial temperature range of 0°C to +70°C. The AD713A and AD713B are rated over the industrial temperature of –40°C to +85°C. The AD713S and AD713T are rated over the military temperature range of –55°C to +125°C and are available processed to MIL-STD-883B, Rev. C.

CONNECTION DIAGRAMS



The AD713 is offered in a 16-pin SOIC, 14-pin plastic DIP and hermetic cerdip package, or in chip form.

PRODUCT HIGHLIGHTS

1. The AD713 is a high speed BiFET op amp that offers excellent performance at competitive prices. It upgrades the performance of circuits using op amps such as the TL074/TL084, LT1058, LF347 and OPA404.
2. Slew rate is 100% tested for a guaranteed minimum of 16 V/μs (J, A and S Grades).
3. The combination of Analog Devices' advanced processing technology, laser wafer drift trimming and well-matched ion-implanted JFETs provides outstanding dc precision. Input offset voltage, input bias current and input offset current are specified in the warmed-up condition and are 100% tested.
4. Very close matching of ac characteristics between the four amplifiers makes the AD713 ideal for high quality active filter applications.

REV. B

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AD713–SPECIFICATIONS (V_S = ±15 V @ T_A = +25°C unless otherwise noted)

Parameter	Conditions	AD713J/A/S Min	Typ	Max	AD713K/B/T Min	Typ	Max	Units
INPUT OFFSET VOLTAGE[1]								
Initial Offset			0.3	**1.5**		0.2	**0.5**	mV
Offset	T_{MIN} to T_{MAX}		0.5	2/2/**2**		0.4	**0.7**/**0.7**/**1.0**	mV
vs. Temp			5			5	20/**20**/**15**	μV/°C
vs. Supply		**78**	95		**84**	100		dB
vs. Supply	T_{MIN} to T_{MAX}	76/76/**76**	95		**84**	100		dB
Long-Term Stability			15			15		μV/Month
INPUT BIAS CURRENT[2]	V_{CM} = 0 V		40	**150**		40	**75**	pA
	V_{CM} = 0 V @ T_{MAX}			3.4/9.6/154			1.7/4.8/77	nA
	V_{CM} = ±10 V		55	200		55	**120**	pA
INPUT OFFSET CURRENT	V_{CM} = 0 V		10	**75**		10	**35**	pA
	V_{CM} = 0 V @ T_{MAX}			1.7/4.8/77			0.8/2.2/36	nA
MATCHING CHARACTERISTICS								
Input Offset Voltage			0.5	**1.8**		0.4	**0.8**	mV
Input Offset Voltage	T_{MIN} to T_{MAX}		0.7	2.3/2.3/**2.3**		0.6	**1.0**/**1.0**/**1.3**	mV
Input Offset Voltage Drift			8			6	25	μV/°C
Input Bias Current			10	**100**		10	**35**	pA
Crosstalk	f = 1 kHz			–130			–130	dB
	f = 100 kHz			–95			–95	dB
FREQUENCY RESPONSE								
Small Signal Bandwidth	Unity Gain	3.0	4.0		3.4	4.0		MHz
Full Power Response	V_O = 20 V p-p		200			200		kHz
Slew Rate	Unity Gain	**16**	20		**18**	20		V/μs
Settling Time to 0.01%			1.0	1.2		1.0	1.2	μs
Total Harmonic Distortion	f = 1 kHz; R_L ≥ 2 kΩ; V_O = 3 V rms		0.0003			0.0003		%
INPUT IMPEDANCE								
Differential			$3\times10^{12}\|5.5$			$3\times10^{12}\|5.5$		Ω‖pF
Common Mode			$3\times10^{12}\|5.5$			$3\times10^{12}\|5.5$		Ω‖pF
INPUT VOLTAGE RANGE								
Differential[3]			±20			±20		V
Common-Mode Voltage[4]			+14.5, –11.5			+14.5, –11.5		V
	T_{MIN} to T_{MAX}	–11		+13	**–11**		+13	V
Common Mode	V_{CM} = ±10 V	**78**	88		**84**	94		dB
Rejection Ratio	T_{MIN} to T_{MAX}	76/76/**76**	84		**82**	90		dB
	V_{CM} = ±11 V	**72**	84		**78**	90		dB
	T_{MIN} to T_{MAX}	70/70/**70**	80		**74**	84		dB
INPUT VOLTAGE NOISE	0.1 Hz to 10 Hz		2			2		μV p-p
	f = 10 Hz		45			45		nV/√Hz
	f = 100 Hz		22			22		nV/√Hz
	f = 1 kHz		18			18		nV/√Hz
	f = 10 kHz		16			16		nV/√Hz
INPUT CURRENT NOISE	f = 1 kHz		0.01			0.01		pA/√Hz
OPEN-LOOP GAIN	V_O = ±10 V; R_L ≥ 2 kΩ	**150**	400		**200**	400		V/mV
	T_{MIN} to T_{MAX}	100/100/**100**			**100**			V/mV
OUTPUT CHARACTERISTICS								
Voltage	R_L ≥ 2 kΩ	+13, –12.5	+13.9, –13.3		+13, –12.5	+13.9, –13.3		V
	T_{MIN} to T_{MAX}	±12/±12/**±12**	+13.8, –13.1		**±12**	+13.8, –13.1		V
Current	Short Circuit		25			25		mA
POWER SUPPLY								
Rated Performance			±15			±15		V
Operating Range		**±4.5**		**±18**	**±4.5**		**±18**	V
Quiescent Current			10.0	**13.5**		10.0	**12.0**	mA
TRANSISTOR COUNT	# of Transistors		120			120		

NOTES

[1]Input Offset Voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.

[2]Bias Current specifications are guaranteed maximum at either input after 5 minutes of operation at T_A = +25°C. For higher temperatures, the current doubles every 10°C.

[3]Defined as voltage between inputs, such that neither exceeds ±10 V from ground.

[4]Typically exceeding –14.1 V negative common-mode voltage on either input results in an output phase reversal.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1, 2]

Supply Voltage . . . . ±18 V
Internal Power Dissipation[2]
Input Voltage[3] . . . . ±18 V
Output Short Circuit Duration
(For One Amplifier) . . . . Indefinite
Differential Input Voltage . . . . $+V_S$ and $-V_S$
Storage Temperature Range (Q) . . . . –65°C to +150°C
Storage Temperature Range (N, R) . . . . –65°C to +125°C
Operating Temperature Range
AD713J/K . . . . 0°C to +70°C
AD713A/B . . . . –40°C to +85°C
AD713S/T . . . . –55°C to +125°C
Lead Temperature Range (Soldering 60 sec) . . . . +300°C

NOTES

[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]Thermal Characteristics:
14-Pin Plastic Package: θ_{JC} = 30°C/Watt; θ_{JA} = 100°C/Watt
14-Pin Cerdip Package: θ_{JC} = 30°C/Watt; θ_{JA} = 110°C/Watt
16-Pin SOIC Package: θ_{JC} = 30°C/Watt; θ_{JA} = 100°C/Watt

[3]For supply voltages less than ±18 V, the absolute maximum input voltage is equal to the supply voltage.

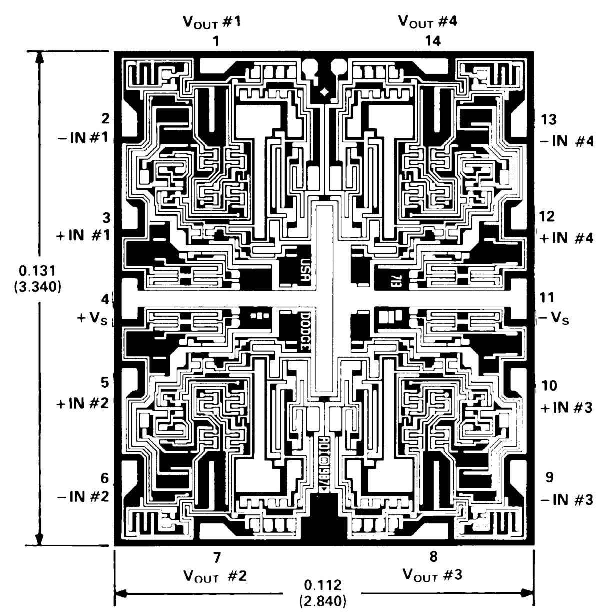
ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD713AQ	–40°C to +85°C	14-Pin Ceramic DIP	Q-14
AD713BQ	–40°C to +85°C	14-Pin Ceramic DIP	Q-14
AD713JCHIPS	0°C to +70°C	Bare Die	
AD713JN	0°C to +70°C	14-Pin Plastic DIP	N-14
AD713JR-16	0°C to +70°C	16-Pin Plastic SOIC	R-16
AD713JR-16-REEL	0°C to +70°C	16-Pin Plastic SOIC	R-16
AD713JR-16-REEL7	0°C to +70°C	16-Pin Plastic SOIC	R-16
AD713KN	0°C to +70°C	14-Pin Plastic DIP	N-14
AD713SCHIPS	–55°C to +125°C	Bare Die	
AD713SQ	–55°C to +125°C	14-Pin Ceramic DIP	Q-14
AD713SQ/883B	–55°C to +125°C	14-Pin Ceramic DIP	Q-14
AD713TQ	–55°C to +125°C	14-Pin Ceramic DIP	Q-14
AD713TQ/883B	–55°C to +125°C	14-Pin Ceramic DIP	Q-14
5962-9063301MCA	–55°C to +125°C	14-Pin Ceramic DIP	Q-14
5962-9063302MCA	–55°C to +125°C	14-Pin Ceramic DIP	Q-14

*N = Plastic DIP; Q = Cerdip; R = Small Outline IC (SOIC).

METALIZATION PHOTOGRAPH

Dimensions shown in inches and (mm).
Contact factory for latest dimensions.



AD713–Typical Characteristics

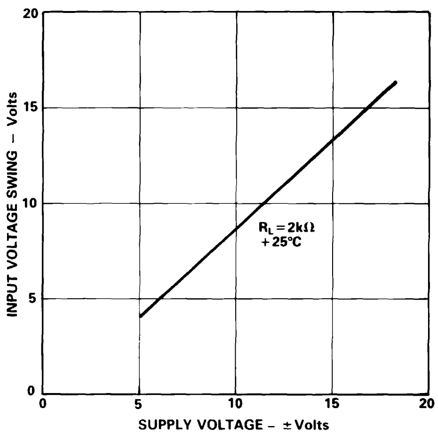


Figure 1. Input Voltage Swing vs. Supply Voltage

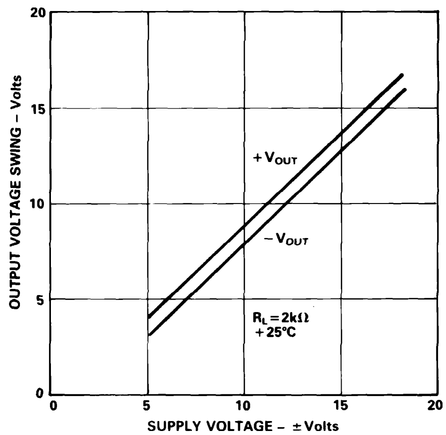


Figure 2. Output Voltage Swing vs. Supply Voltage

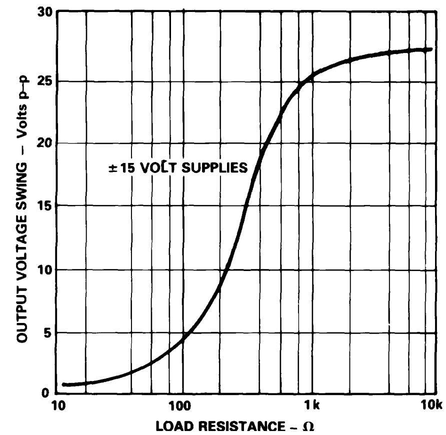


Figure 3. Output Voltage Swing vs. Load Resistance

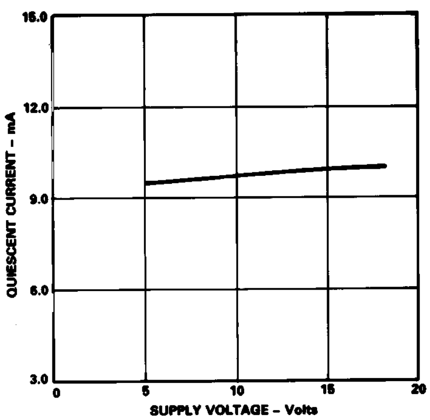


Figure 4. Quiescent Current vs. Supply Voltage

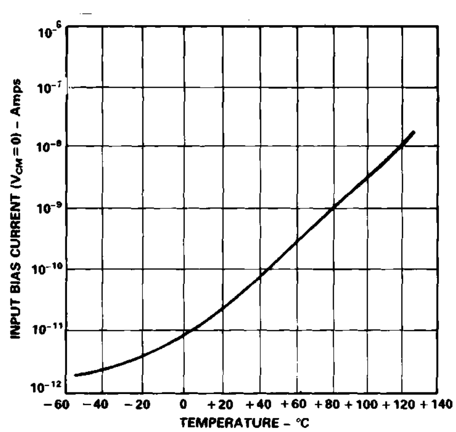


Figure 5. Input Bias Current vs. Temperature

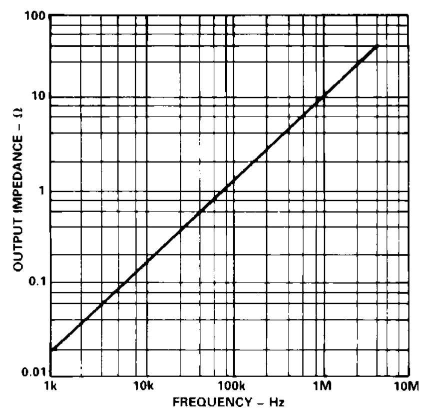


Figure 6. Output Impedance vs. Frequency, G = 1

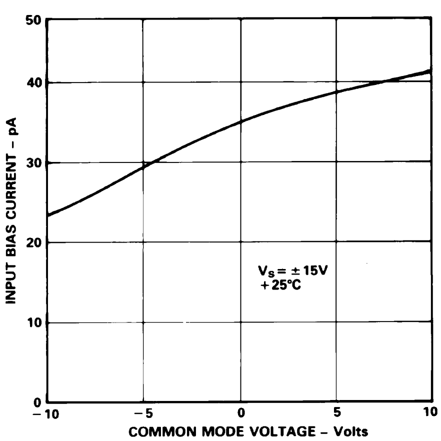


Figure 7. Input Bias Current vs. Common Mode Voltage

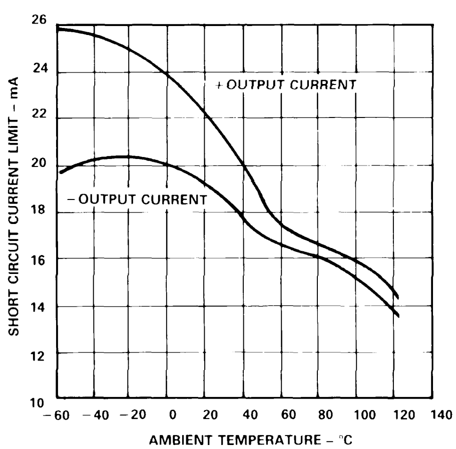


Figure 8. Short Circuit Current Limit vs. Temperature

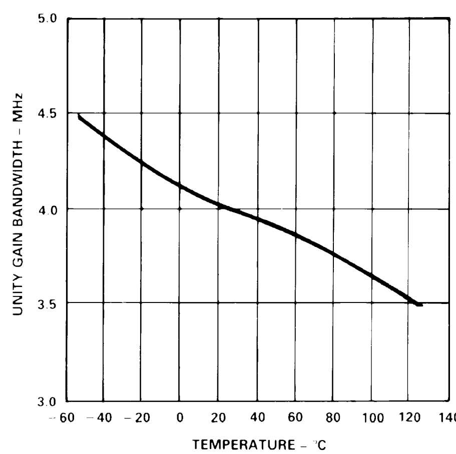


Figure 9. Gain Bandwidth Product vs. Temperature

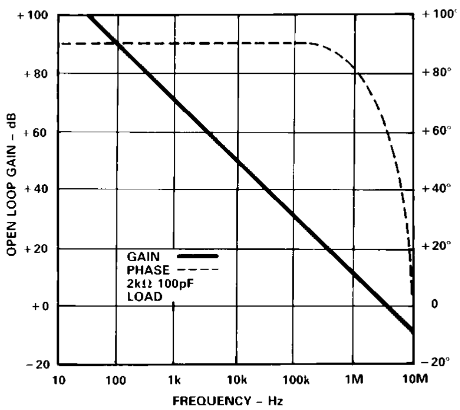


Figure 10. Open-Loop Gain and Phase Margin vs. Frequency

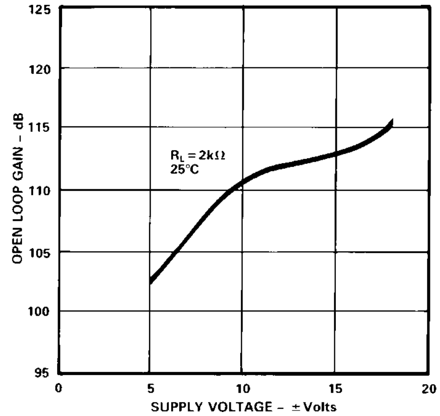


Figure 11. Open-Loop Gain vs. Supply Voltage

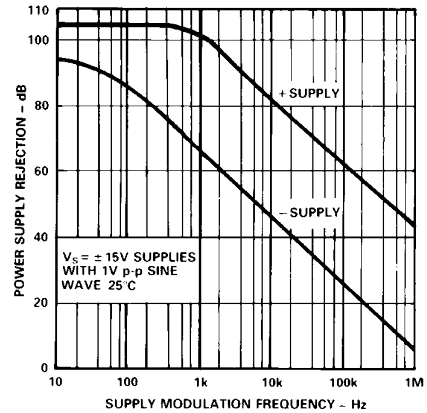


Figure 12. Power Supply Rejection vs. Frequency

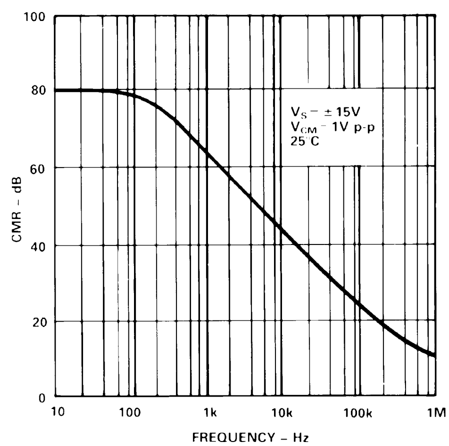


Figure 13. Common Mode Rejection vs. Frequency

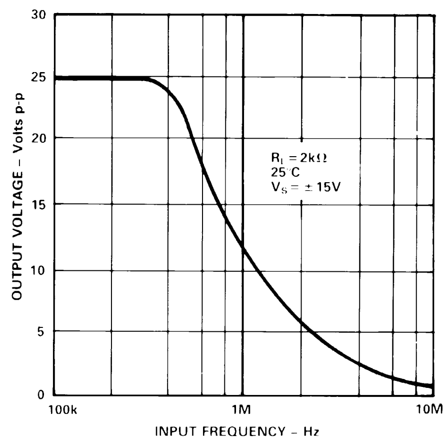


Figure 14. Large Signal Frequency Response

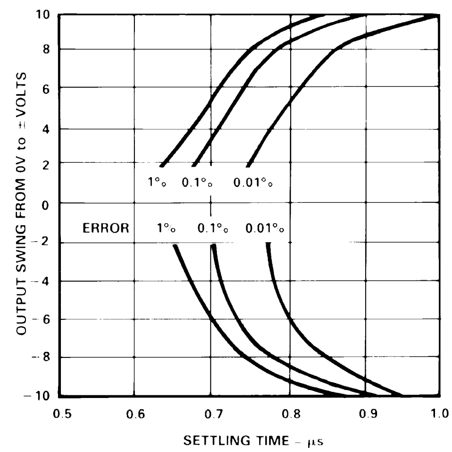


Figure 15. Output Swing and Error vs. Settling Time

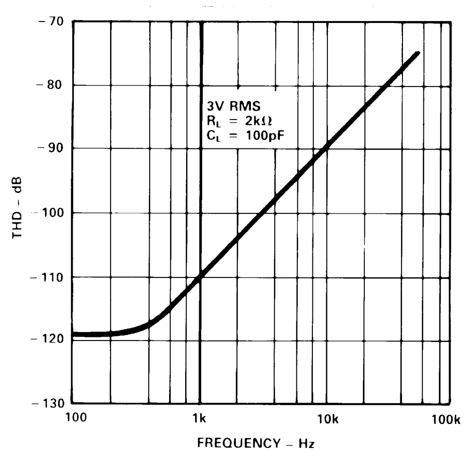


Figure 16. Total Harmonic Distortion vs. Frequency

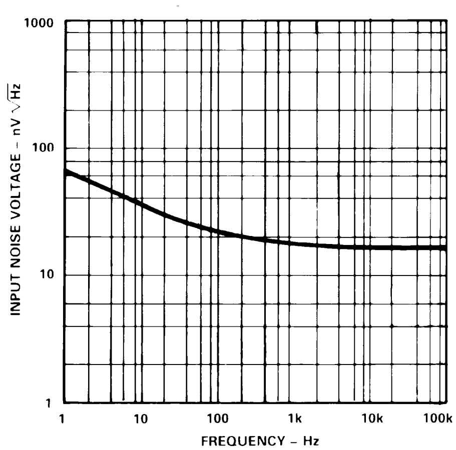


Figure 17. Input Noise Voltage Spectral Density

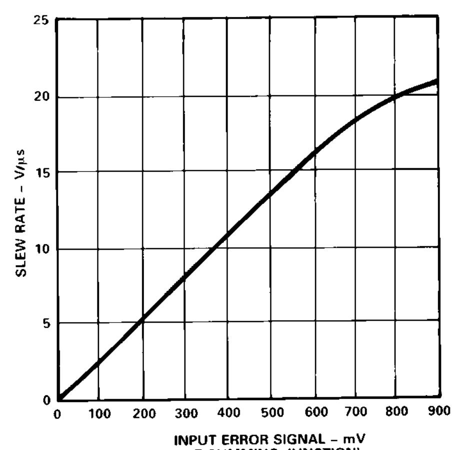
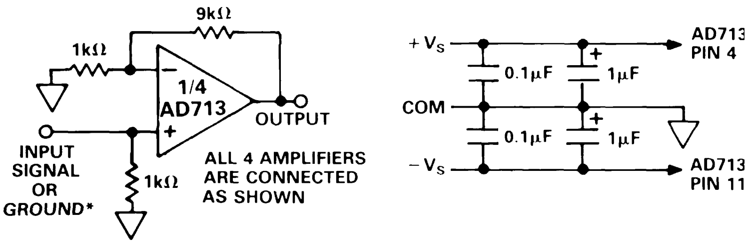


Figure 18. Slew Rate vs. Input Error Signal



*THE SIGNAL INPUT (1kHz SINEWAVE, 2V p-p) IS APPLIED TO ONE AMPLIFIER AT A TIME. THE OUTPUTS OF THE OTHER THREE AMPLIFIERS ARE THEN MEASURED FOR CROSSTALK.

Figure 19. Crosstalk Test Circuit

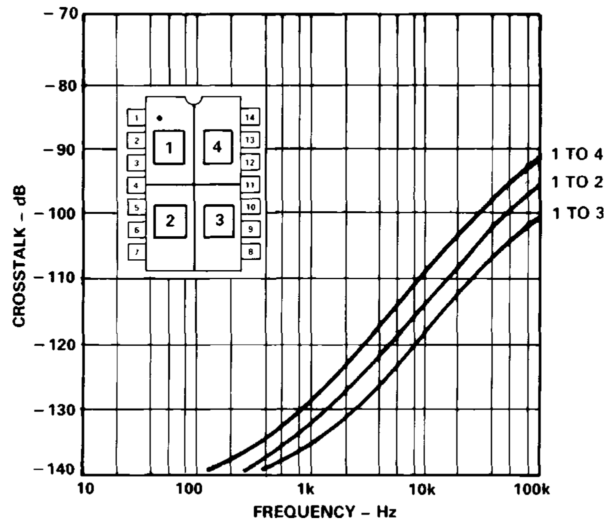


Figure 20. Crosstalk vs. Frequency

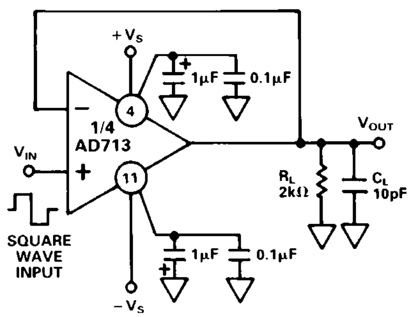


Figure 21a. Unity Gain Follower

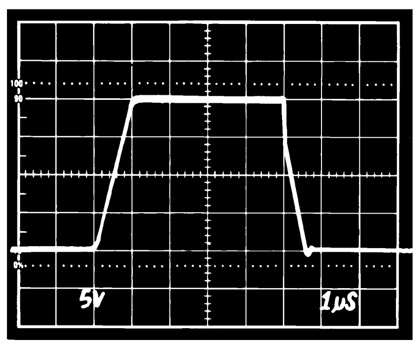


Figure 21b. Unity Gain Follower Pulse Response (Large Signal)

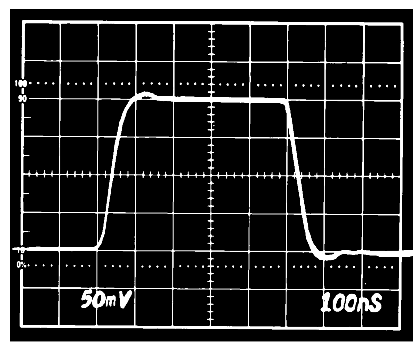


Figure 21c. Unity Gain Follower Pulse Response (Small Signal)

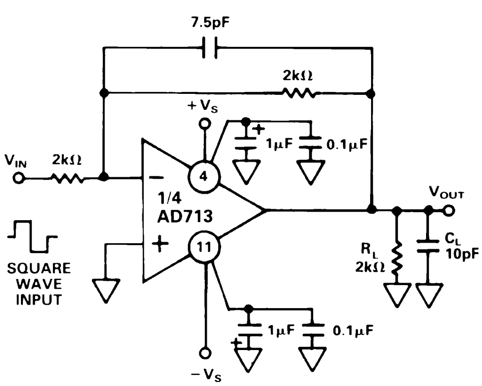


Figure 22a. Unity Gain Inverter

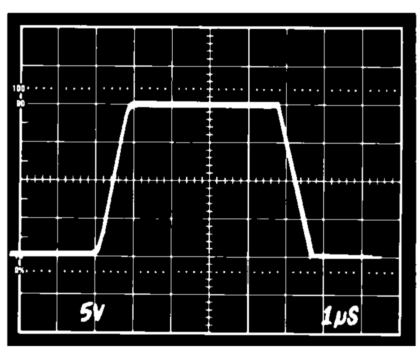


Figure 22b. Unity Gain Inverter Pulse Response (Large Signal)

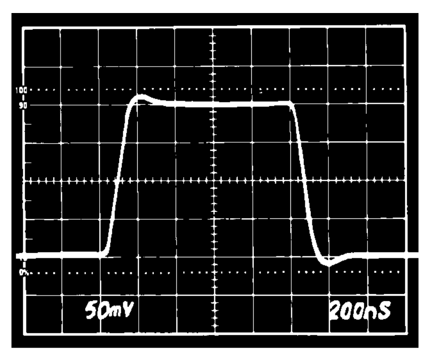


Figure 22c. Unity Gain Inverter Pulse Response (Small Signal)

MEASURING AD713 SETTLING TIME

The photos of Figures 24 and 25 show the dynamic response of the AD713 while operating in the settling time test circuit of Figure 23. The input of the settling time fixture is driven by a flat-top pulse generator. The error signal output from the false summing node of A1, the AD713 under test, is clamped, amplified by op amp A2 and then clamped again.

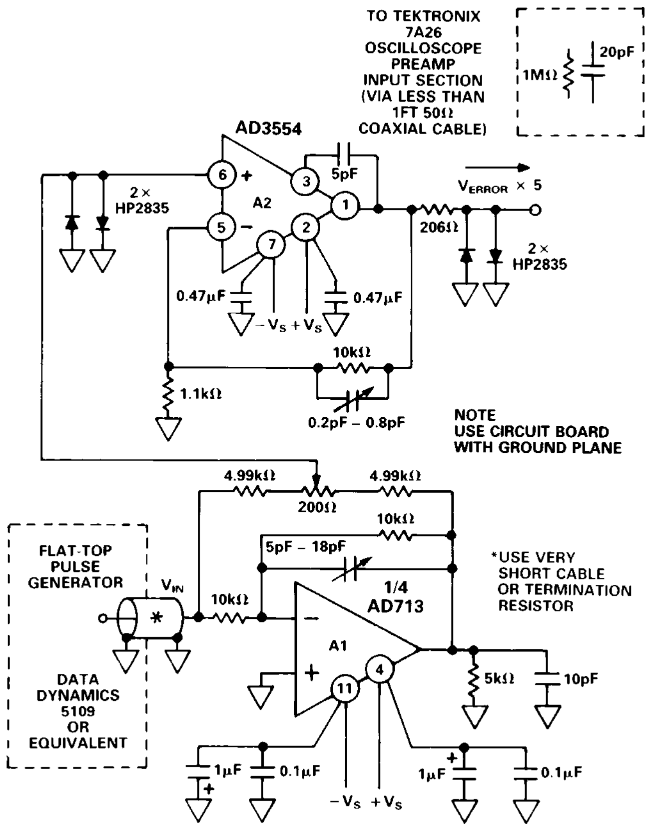


Figure 23. Settling Time Test Circuit

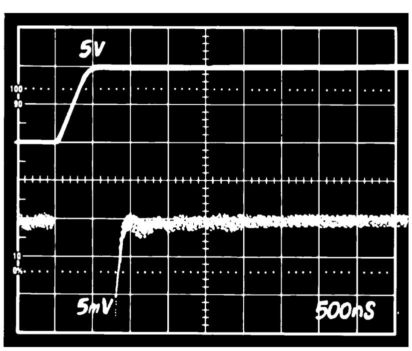


Figure 24. Settling Characteristics 0 V to +10 V Step. Upper Trace: Output of AD713 Under Test (5 V/div). Lower Trace: Amplified Error Voltage (0.01%/div)

The error signal is thus clamped twice: once to prevent overloading amplifier A2 and then a second time to avoid overloading the oscilloscope preamp. A Tektronix oscilloscope preamp type 7A26 was carefully chosen because it recovers from the approximately 0.4 volt overload quickly enough to allow accurate measurement of the AD713's 1 µs settling time. Amplifier A2 is a very high speed FET input op amp; it provides a voltage gain of 10, amplifying the error signal output of the AD713 under test (providing an overall gain of 5).

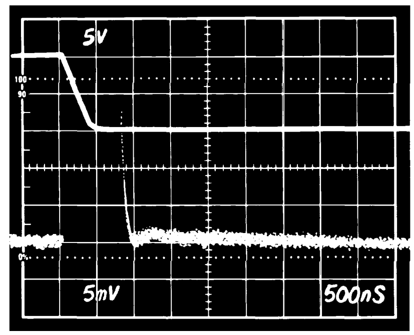


Figure 25. Settling Characteristics to –10 V Step. Upper Trace: Output of AD713 Under Test (5 V/div). Lower Trace: Amplified Error Voltage (0.01%/ div)

POWER SUPPLY BYPASSING

The power supply connections to the AD713 must maintain a low impedance to ground over a bandwidth of 4 MHz or more. This is especially important when driving a significant resistive or capacitive load, since all current delivered to the load comes from the power supplies. Multiple high quality bypass capacitors are recommended for each power supply line in any critical application. A 0.1 µF ceramic and a 1 µF electrolytic capacitor as shown in Figure 26 placed as close as possible to the amplifier (with short lead lengths to power supply common) will assure adequate high frequency bypassing in most applications. A minimum bypass capacitance of 0.1 µF should be used for any application.

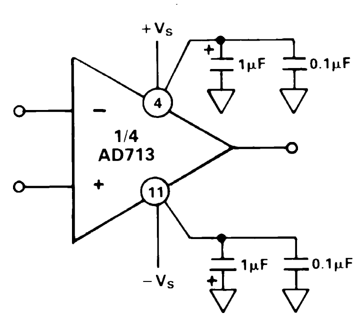


Figure 26. Recommended Power Supply Bypassing

A HIGH SPEED INSTRUMENTATION AMPLIFIER CIRCUIT

The instrumentation amplifier circuit shown in Figure 27 can provide a range of gains from unity up to 1000 and higher using only a single AD713. The circuit bandwidth is 1.2 MHz at a gain of 1 and 250 kHz at a gain of 10; settling time for the entire circuit is less than 5 µs to within 0.01% for a 10 volt step, (G = 10). Other uses for amplifier A4 include an active data guard and an active sense input.

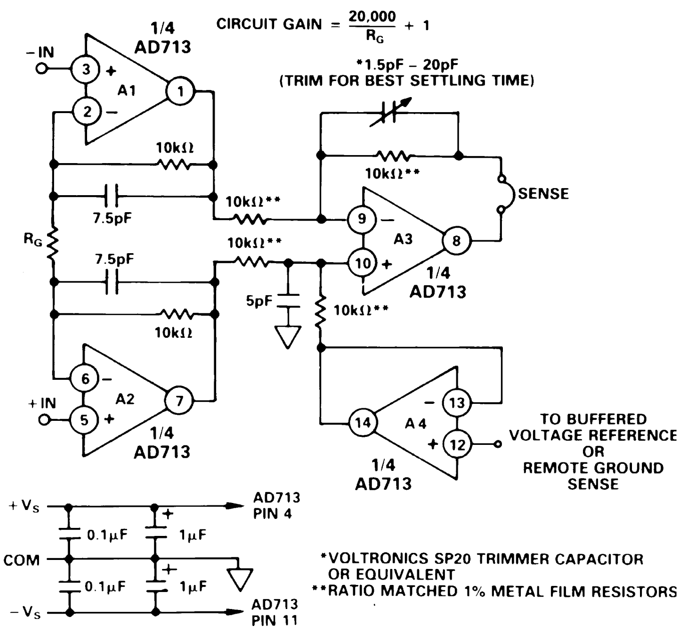


Figure 27. A High Speed Instrumentation Amplifier Circuit

Table I provides a performance summary for this circuit. The photo of Figure 28 shows the pulse response of this circuit for a gain of 10.

Table I. Performance Summary for the High Speed Instrumentation Amplifier Circuit

Gain	R_G	Bandwidth	T Settle (0.01%)
1	NC	1.2 MHz	2 µs
2	20 kΩ	1.0 MHz	2 µs
10	4.04 kΩ	0.25 MHz	5 µs

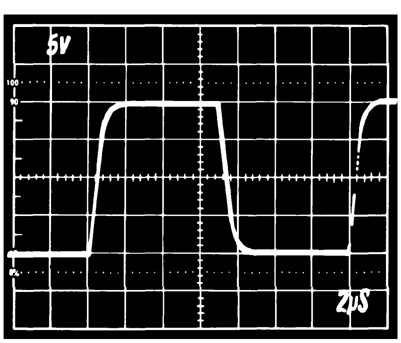


Figure 28. The Pulse Response of the High Speed Instrumentation Amplifier. Gain = 10

A HIGH SPEED FOUR OP AMP CASCADED AMPLIFIER CIRCUIT

Figure 29 shows how the four amplifiers of the AD713 may be connected in cascade to form a high gain, high bandwidth amplifier. This gain of 100 amplifier has a –3 dB bandwidth greater than 600 kHz.

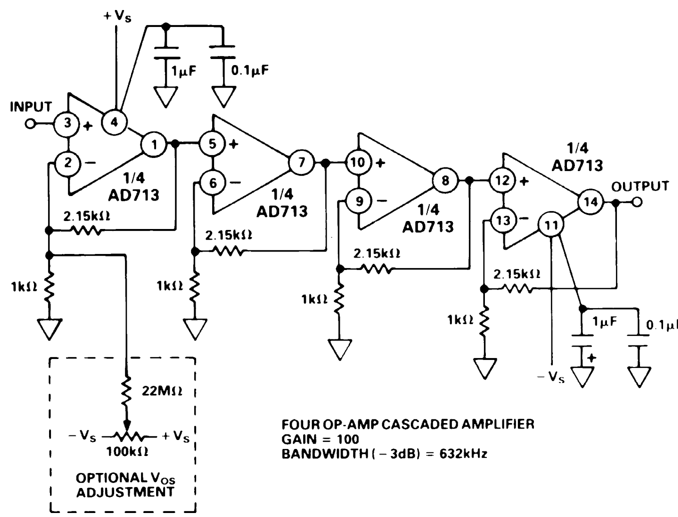


Figure 29. A High Speed Four Op Amp Cascaded Amplifier Circuit

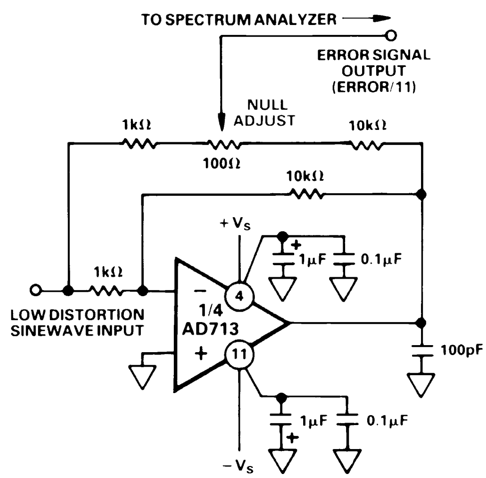


Figure 30. THD Test Circuit

HIGH SPEED OP AMP APPLICATIONS AND TECHNIQUES

DAC Buffers (I-to-V Converters)

The wide input dynamic range of JFET amplifiers makes them ideal for use in both waveform reconstruction and digital-audio DAC applications. The AD713, in conjunction with the AD1860 DAC, can achieve 0.0016% THD (here at a 4fs or a 176.4 kHz update rate) without requiring the use of a deglitcher. Just such a circuit is shown in Figure 31. The 470 pF feedback capacitor used with IC2a, along with op amp IC2b and its associated components, together form a 3-pole low-pass filter. Each or all of these poles can be tailored for the desired attenuation and phase characteristics required for a particular application. In this application, one half of an AD713 serves each channel in a two-channel stereo system.

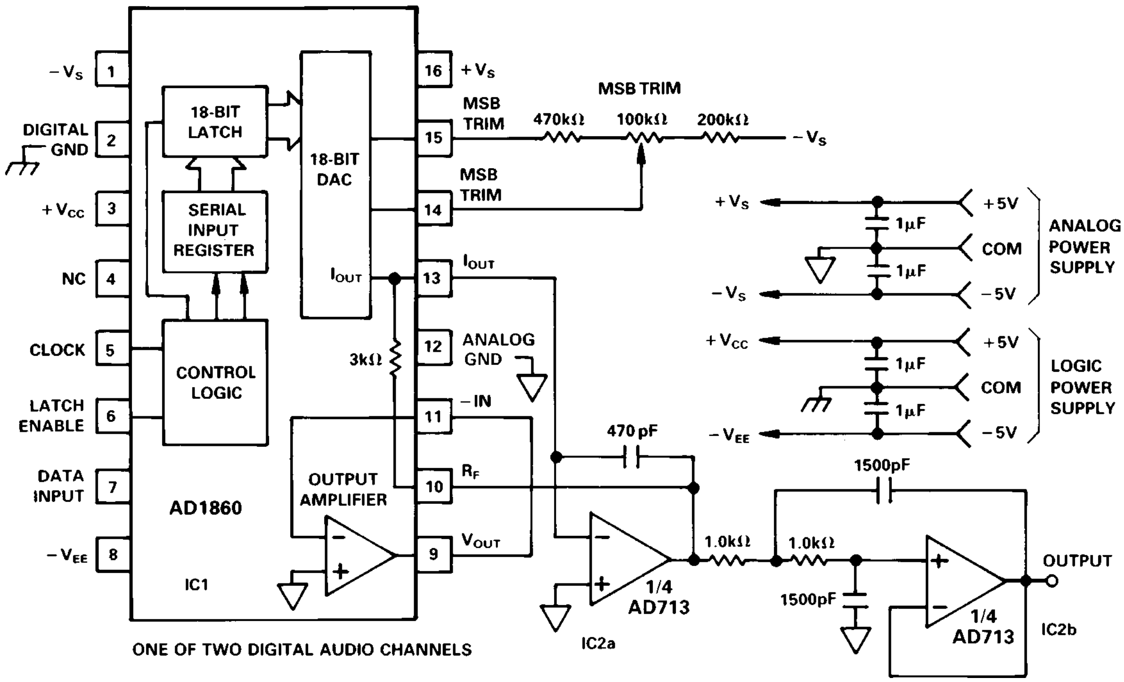


Figure 31. A D/A Converter Circuit for Digital Audio

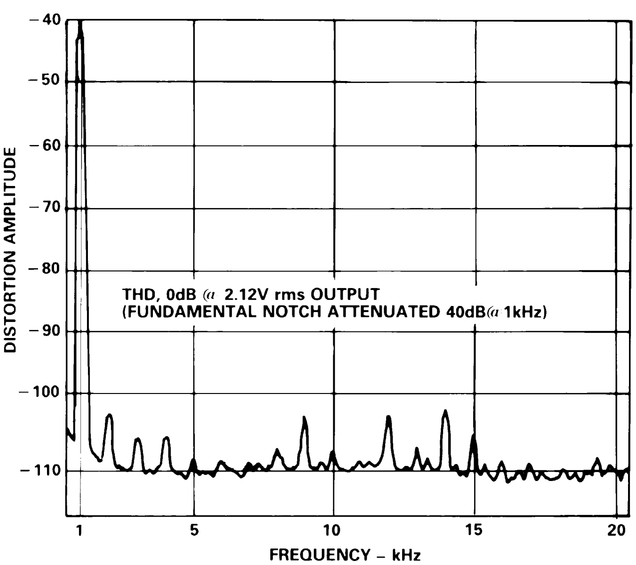


Figure 32. Harmonic Distortion as Frequency for the Digital Audio Circuit of Figure 31

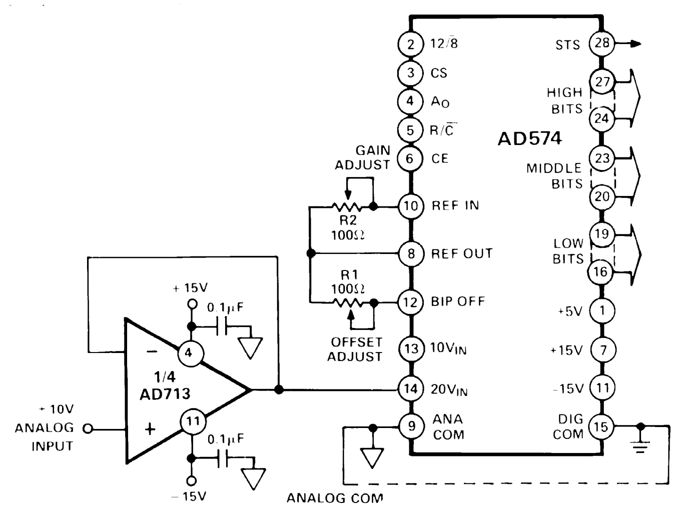


Figure 33. The AD713 as an ADC Buffer

Driving the Analog Input of an A/D Converter

An op amp driving the analog input of an A/D converter, such as that shown in Figure 33, must be capable of maintaining a constant output voltage under dynamically changing load conditions. In successive approximation converters, the input current is compared to a series of switched trial currents. The comparison point is diode clamped but may vary by several hundred millivolts, resulting in high frequency modulation of the A/D input current. The output impedance of a feedback amplifier is made artificially low by its loop gain. At high frequencies, where the loop gain is low, the amplifier output impedance can approach its open loop value.

Most IC amplifiers exhibit a minimum open loop output impedance of 25 Ω, due to current limiting resistors. A few hundred microamps reflected from the change in converter loading can introduce errors in instantaneous input voltage. If the A/D conversion speed is not excessive and the bandwidth of the amplifier is sufficient, the amplifier's output will return to the nominal value before the converter makes its comparison. However, many amplifiers have relatively narrow bandwidths, yielding slow recovery from output transients. The AD713 is ideally suited as a driver for A/D converters since it offers both a wide bandwidth and a high open loop gain.

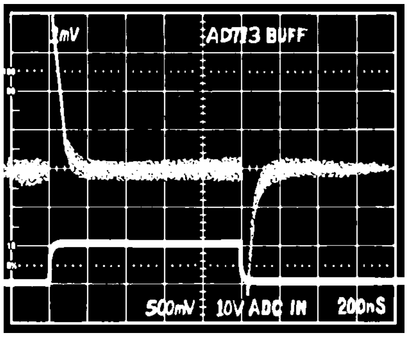


Figure 34. Buffer Recovery Time Source Current = 2 mA

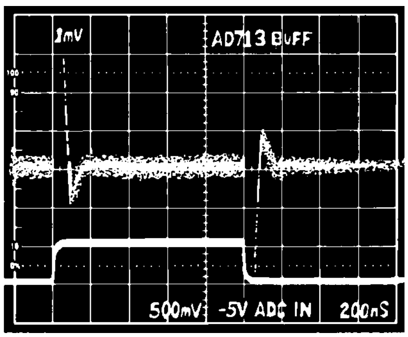


Figure 35. Buffer Recovery Time Sink Current = 1 mA

Driving A Large Capacitive Load

The circuit of Figure 36 employs a 100 Ω isolation resistor which enables the amplifier to drive capacitive loads exceeding 1500 pF; the resistor effectively isolates the high frequency feedback from the load and stabilizes the circuit. Low frequency feedback is returned to the amplifier summing junction via the low pass filter formed by the 100 Ω series resistor and the load capacitance, C1. Figure 37 shows a typical transient response for this connection.

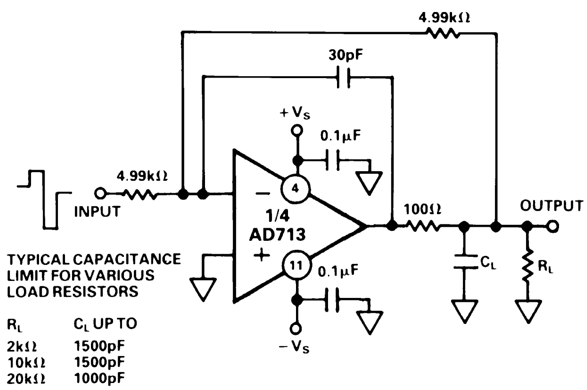


Figure 36. Circuit for Driving a Large Capacitance Load

Table II. Recommended Trim Resistor Values vs. Grades for AD7545 for V_D = +5 V

Trim Resistor	JN/AQ/ SD	KN/BQ/ TD	LN/CQ/ UD	GLN/GCQ/ GUD
R1	500 Ω	200 Ω	100 Ω	20 Ω
R2	150 Ω	68 Ω	33 Ω	6.8 Ω

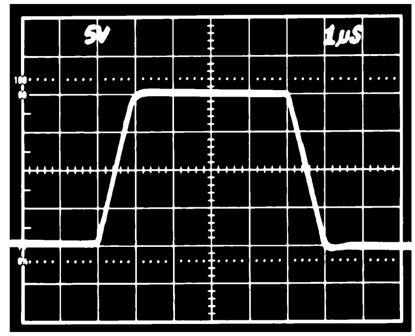


Figure 37. Transient Response, R_L = 2 kΩ, C_L = 500 pF

CMOS DAC APPLICATIONS

The AD713 is an excellent output amplifier for CMOS DACs. It can be used to perform both 2 and 4 quadrant operation. The output impedance of a DAC using an inverted R-2R ladder approaches R for codes containing many "1"s, 3R for codes containing a single "1" and infinity for codes containing all zeros.

For example, the output resistance of the AD7545 will modulate between 11 kΩ and 33 kΩ. Therefore, with the DAC's internal feedback resistance of 11 kΩ, the noise gain will vary from 2 to 4/3. This changing noise gain modulates the effect of the input offset voltage of the amplifier, resulting in nonlinear DAC amplifier performance. The AD713, with its guaranteed 1.5 mV input offset voltage, minimizes this effect achieving 12-bit performance.

Figures 38 and 39 show the AD713 and a 12-bit CMOS DAC, the AD7545, configured for either a unipolar binary (2-quadrant multiplication) or bipolar (4-quadrant multiplication) operation. Capacitor C1 provides phase compensation which reduces overshoot and ringing.

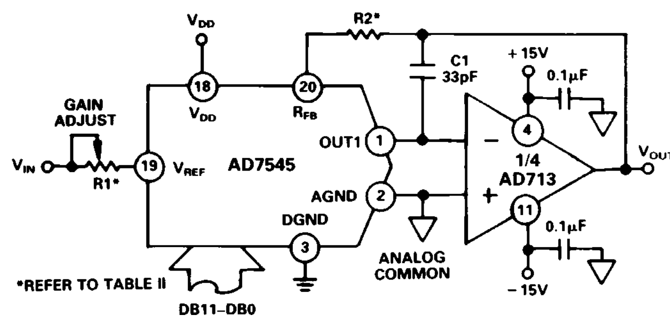


Figure 38. Unipolar Binary Operation

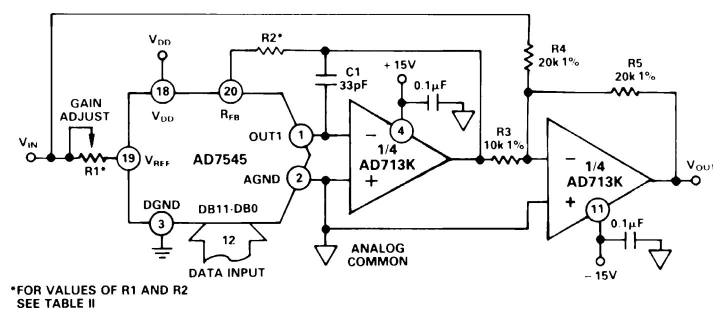
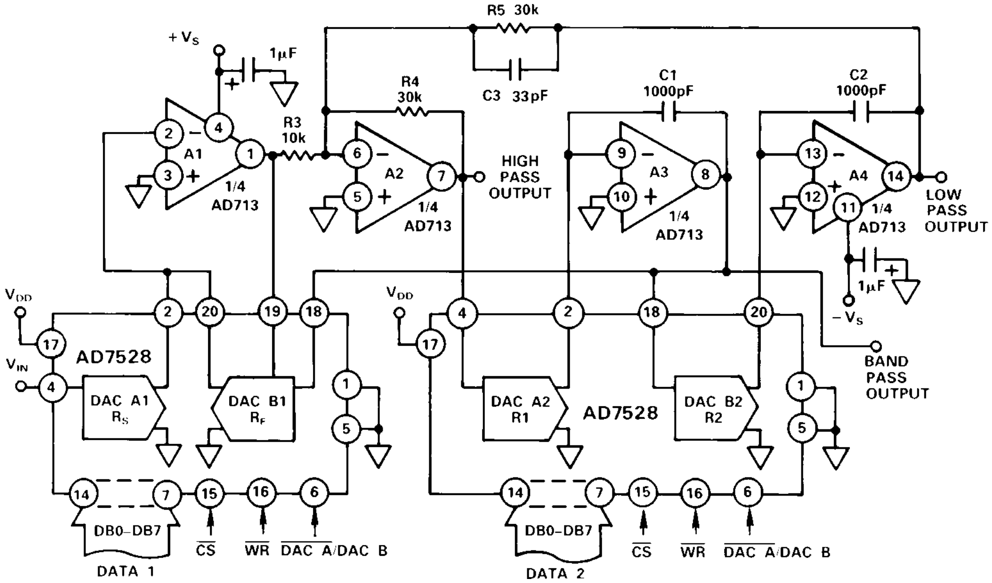


Figure 39. Bipolar Operation



CIRCUIT EQUATIONS

$C_1 = C_2,\ R_1 = R_2,\ R_4 = R_5$

$$f_C = \frac{1}{2\pi\ R_1\ C_1}$$

$$Q = \frac{R_3}{R_4} \cdot \frac{R_F}{R_{FBB1}}$$

$$A_O = -\ \frac{R_F}{R_S}$$

Note:
DAC equivalent resistance equals

$$\frac{256 \times (\text{DAC Ladder resistance})}{\text{DAC Digital Code}}$$

Figure 40. A Programmable State Variable Filter Circuit

FILTER APPLICATIONS

A Programmable State Variable Filter

For the state variable or universal filter configuration of Figure 40 to function properly, DACs A1 and B1 need to control the gain and Q of the filter characteristic, while DACs A2 and B2 must accurately track for the simple expression of f_C to be true. This is readily accomplished using two AD7528 DACs and one AD713 quad op amp. Capacitor C3 compensates for the effects of op amp gain-bandwidth limitations.

This filter provides low pass, high pass and band pass outputs and is ideally suited for applications where microprocessor control of filter parameters is required. The programmable range for component values shown is f_C = 0 to 15 kHz and Q = 0.3 to 4.5.

GIC and FDNR FILTER APPLICATIONS

The closely matched and uniform ac characteristics of the AD713 make it ideal for use in GIC (gyrator) and FDNR (frequency dependent negative resistor) filter applications. Figures 41 and 43 show the AD713 used in two typical active filters. The first shows a single AD713 simulating two coupled inductors configured as a one-third octave bandpass filter. A single section of this filter meets ANSI class II specifications and handles a 7.07 V rms signal with <0.002% THD (20 Hz–20 kHz).

Figure 43 shows a 7-pole antialiasing filter for a 2 × oversampling (88.2 kHz) digital audio application. This filter has <0.05 dB pass band ripple and 19.8 ±0.3 µs delay,
dc-20 kHz and will handle a 5 V rms signal (V_S = ±15 V) with no overload at any internal nodes.

The filter of Figure 41 can be scaled for any center frequency by using the formula:

$$f_C = \frac{1.11}{2\pi RC}$$

where all resistors and capacitors scale equally. Resistors R3–R8 should not be greater than 2 kΩ in value, to prevent parasitic oscillations caused by the amplifier's input capacitance.

$$f_c = \frac{1.11}{2\pi RC}$$

$$C_1 = C_2 = C_3 = C_4 = C$$

$$R_1 = R_2 = 4.76R$$

$$R_{11} = 4.32R$$

$$R_3 = R_4 = R_5 = R_6 = R_7 = R_8 = R_9 = R_{10} = R$$

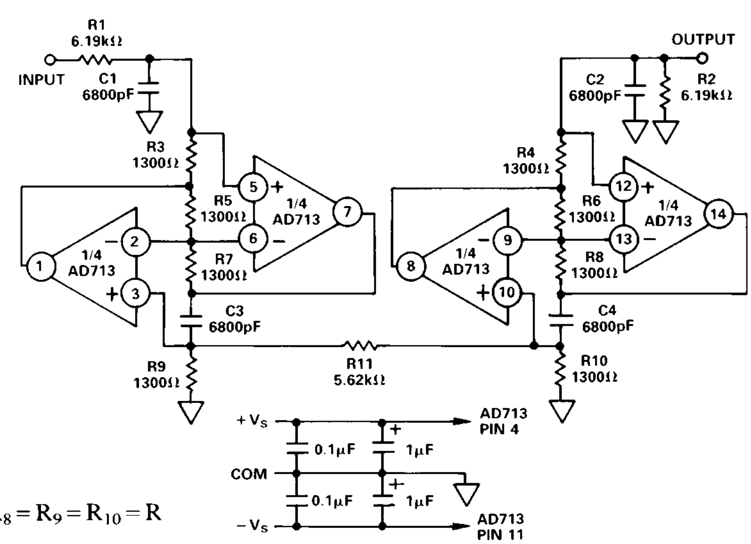


Figure 41. A 1/3 Octave Filter Circuit

If this is not practical, small lead capacitances (10–20 pF) should be added across R5 and R6. Figures 42 and 44 show the output amplitude vs. frequency of these filters.

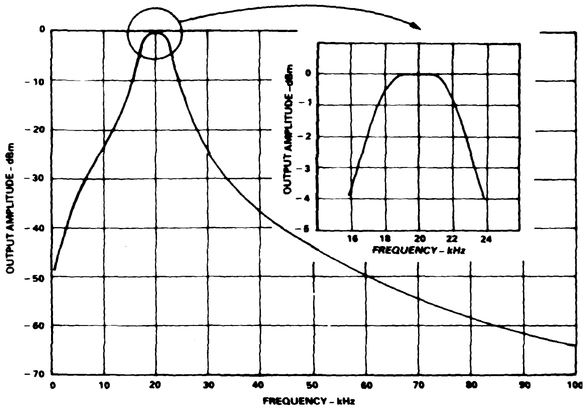


Figure 42. Output Amplitude vs. Frequency of 1/3 Octave Filter

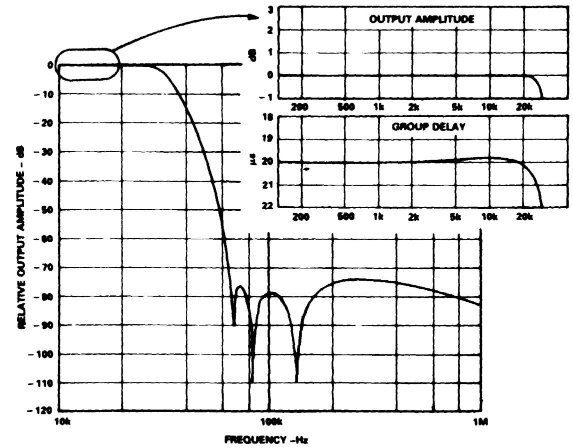


Figure 44. Relative Output Amplitude vs. Frequency of Antialiasing Filter

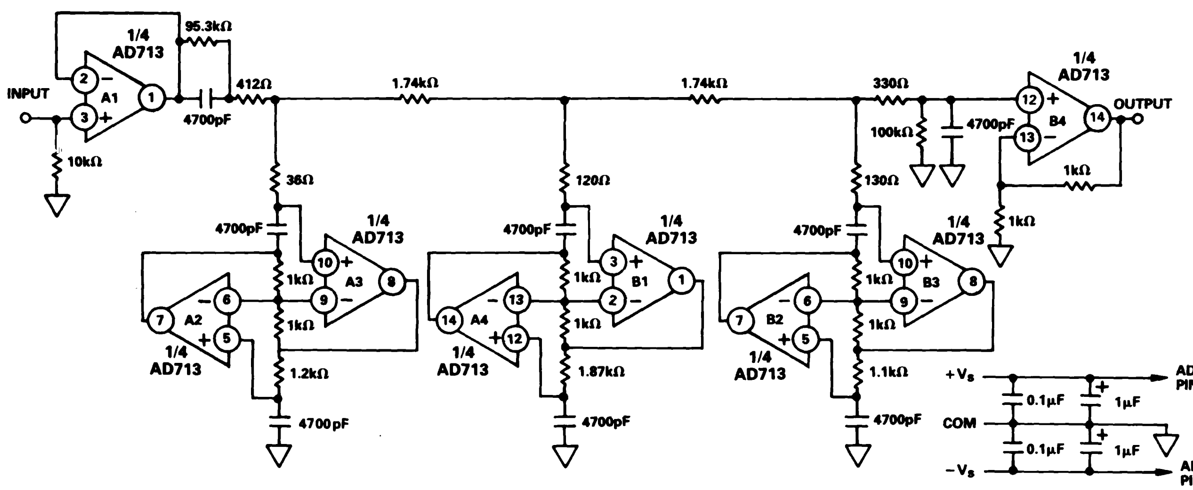
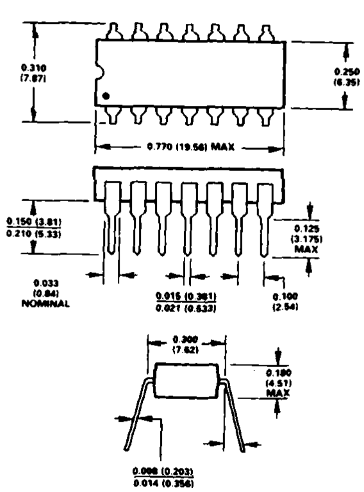


Figure 43. An Antialiasing Filter

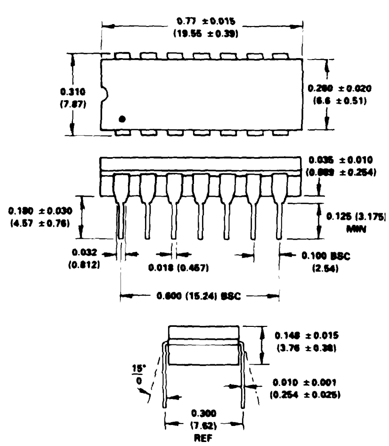
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

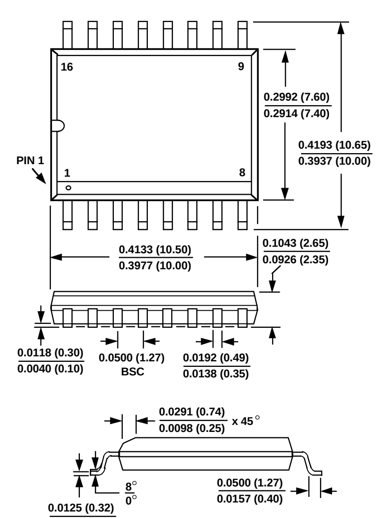
14-Pin Plastic (N-14A) DIP Package



14-Pin Cerdip (Q-14) Package



16-Pin SOIC (R-16) Package



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